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EXAMINER	
CERVETTI, DAVID GARCIA	
ART UNIT	**PAPER NUMBER**
2136	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,003	ARAI, YOSHIHISA	
	Examiner	Art Unit	
	David G. Cervetti	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-18,20-31,33-44,46-57,59-70 and 72-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-18,20-31,33-44,46-57,59-70 and 72-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments filed August 26, 2005, have been fully considered but they are not persuasive.

2. Claims 1-6, 8-18, 20-31, 33-44, 46-57, 59-70, and 72-76 are pending and have been examined. Claims 7,19, 32, 45, 58, and 71 have been cancelled.

Response to Amendment

3. The objection to the drawings is withdrawn. The replacement drawing filed August 26, 2005 is accepted.

4. Assuming arguendo that the combination of the cited prior art does not teach or suggest the claimed invention, Ishida (US Patent Number 5,604,143) teaches that if two points in a circuit are connected, a high level signal is output to a data line, and if two points in a circuit are disconnected, a low level signal is output to a data line. Furthermore, using isolated circuits to generate random numbers was conventional and well known (Krone et al., US Patent Number 6,359,983).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8-9, 20-21, 33-34, 46-47, 59-60, and 72-73 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8-9, 20-21, 33-34, 46-47, 59-60, and 72-73 recite the limitation "according to claim NUMBER" in line 1 of the claim, wherein NUMBER is the cancelled claim in each block. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this document, Examiner has interpreted these claims as being dependent on the independent claim.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1-5, 8-10, 12-17, 20-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa (US Patent Number: 5,117,380), and further in view of Hoffman (US Patent Number: 5,706,218).

Regarding claim 1, Tanagawa teaches an oscillator which generates a clock (figure 1, column 2, lines 1-67); and a counter which operates in synchronism with the clock (column 2, lines 29-55), wherein a count value of said counter is output in response to a signal asynchronous with the clock (column 2, lines 20-50, column 3, 1-45), and the count value is used as an initial value to generate a random number (column 3, lines 45-65, column 4, lines 1-26). Tanagawa does not expressly disclose wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output. However, Hoffman teaches wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output (column 3, lines 1-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically

disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claim 13, Tanagawa teaches an oscillator which generates a clock (figure 1, column 2, lines 1-67); and a counter which operates in synchronism with the clock (column 2, lines 29-55), wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal (column 2, lines 20-50, column 3, 1-45), and the count value is used as an initial value to generate a random number (column 3, lines 45-65, column 4, lines 1-26). Tanagawa does not expressly disclose wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output. However, Hoffman teaches wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output (column 3, lines 1-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claims 2 and 14, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 1 and 13, respectively above. Furthermore, Tanagawa teaches wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 3 and 15, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 1 and 13, respectively above. Furthermore, Tanagawa teaches wherein the signal is an operation start signal output from a controller (column 2, lines 9-20).

Regarding claims 4 and 16, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 3 and 15, respectively above. Furthermore, Tanagawa teaches wherein the operation start signal is output when the controller recognizes that a power supply is turned on (column 2, lines 50-67).

Regarding claims 5 and 17, the combination of Tanagawa and Hoffman does not disclose expressly wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user. However, Examiner takes Official Notice that performing an operation triggered by a user is conventional and well known. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output a signal when a user performs an operation since Examiner takes Official Notice that it was conventional and well known.

Regarding claims 8 and 20, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 1 and 13, respectively above. Furthermore, Hoffman teaches wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal (columns 1-4, figures 1, 3).

Regarding claims 9 and 21, the combination of Tanagawa and Hoffman does not disclose expressly wherein after the count value is output, the clock is used as a system clock. However, Tanagawa teaches the clock being independent from the system clock (column 2, lines 9-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the clock as a system clock after the count value was output. One of ordinary skill in the art would have been motivated to do so because the use of system clocks was well known in the art.

Regarding claims 10 and 22, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 1 and 13, respectively above. Furthermore, Tanagawa teaches wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output (column 3, lines 25-40).

Regarding claims 12 and 24, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 1 and 13, respectively above. Furthermore, Tanagawa teaches wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously

received by the random number generating circuit as the initial value (column 2, lines 40-67, column 3, lines 1-45).

9. Claims 25-31, 33-44, and 46-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Hoffman and Domenik et al. (US Patent Number: 4,694,412, hereinafter "Domenik").

Regarding claim 25, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock (figure 1, column 2, lines 20-50, column 3, 1-45); and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit, wherein a count value of said counter is output in response to a signal asynchronous with the clock (column 2, lines 20-50), the count value is used as the initial value, and transfer data is kept secret using the random number. Tanagawa does not expressly disclose the output count value is used as the initial value, transfer data is kept secret using the random number, or wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output. However, Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65), Domenik teaches encrypting data using the random number (column 3, lines 1-52), and Hoffman teaches wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said

oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output (column 3, lines 1-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output and to keep transfer data secret using the random number. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claim 38, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock (figure 1, column 2, lines 20-50, column 3, 1-45); and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit, wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal (column 2, lines 20-50, column 3, 1-45), the count value is used as the initial value, and transfer data is kept secret using the random number. Tanagawa does not expressly disclose the output count value is used as the initial value, transfer data is kept secret using the random number, or wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said

oscillator and said external terminal are electrically connected after the count value is output. However, Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65), Domenik teaches encrypting data using the random number (column 3, lines 1-52), and Hoffman teaches wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output (column 3, lines 1-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output and to keep transfer data secret using the random number. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claims 26 and 39, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Tanagawa teaches wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 27 and 40, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25and 38, respectively above. Furthermore, Tanagawa teaches wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 28 and 41, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38, respectively above. Furthermore, Tanagawa teaches wherein the signal is an operation start signal output from a controller (column 2, lines 9-20).

Regarding claims 29 and 42, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 28 and 41, respectively above. Furthermore, Tanagawa teaches wherein the operation start signal is output when the controller recognizes that a power supply is turned on (column 2, lines 50-67).

Regarding claims 30 and 43, the combination of Tanagawa, Hoffman, and Domenik does not disclose expressly wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user. However, Examiner takes Official Notice that performing an operation triggered by a user is conventional and well known. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output a signal when a user performs an operation since Examiner takes Official Notice that it was conventional and well known.

Regarding claims 31 and 44, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38, respectively above. Furthermore, Tanagawa teaches that the output occurs only when a high read signal is received (column 2, lines 40-54) and Domenik teaches wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal (column 9, lines 30-67).

Regarding claims 33 and 46, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38, respectively above. Furthermore, Hoffman teaches wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal (columns 1-4, figures 1, 3).

Regarding claims 34 and 47, the combination of Tanagawa, Hoffman, and Domenik does not disclose expressly wherein after the count value is output, the clock is used as a system clock. However, Tanagawa teaches the clock being independent from the system clock (column 2, lines 9-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the clock as a system clock after the count value was output. One of ordinary skill in the art would have been motivated to do so because the use of system clocks was well known in the art.

Regarding claims 35 and 48, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38, respectively above. Furthermore, Tanagawa teaches wherein a timing at which the count value is

output changes within a range of time longer than a period of the clock every time the count value is output (column 3, lines 25-40).

Regarding claims 36 and 49, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38, respectively above. Furthermore, Domenik teaches using a latch circuit (column 6, lines 1-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because using a count value as initial or seed value for a random number generator was well known in the art.

Regarding claims 37 and 50, the combination of Tanagawa, Hoffman, and Domenik teaches the limitations as set forth under claims 25 and 38, respectively above. Furthermore, Tanagawa teaches wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number generating circuit as the initial value (column 2, lines 40-67, column 3, lines 1-45).

10. Claims 51-57, 59-70, and 72-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Maeda et al. (US Patent Number 6,611,907, hereinafter Maeda), Hoffman, and Domenik et al. (US Patent Number: 4,694,412, hereinafter "Domenik").

Regarding claim 51, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock (column 2, lines 20-50, column 3, 1-

45) and a counter which operates in synchronism with the clock (column 2, lines 20-50, column 3, 1-45), and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit (column 2, lines 20-50, column 3, 1-45). Tanagawa does not expressly disclose an SD memory card driven by said driver and having a data protecting function, wherein a count value of said counter is output in response to a signal asynchronous with the clock, the count value is used as the initial value, and transfer data is kept secret using the random number, and wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output. However, Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65); Domenik teaches encrypting data using the random number (column 3, lines 1-52), and Hoffman teaches wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output (column 3, lines 1-65); and Maeda teaches a random number generated by a SD memory card (figures 2A, 2B, 2C, 3A). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said

oscillator and external terminal are electrically connected after the count value is output and to keep transfer data secret using the random number, an SD memory card, and to keep data secret using a random number. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claim 64, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock (column 2, lines 20-50, column 3, 1-45) and a counter which operates in synchronism with the clock (column 2, lines 20-50, column 3, 1-45), and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit (column 2, lines 20-50, column 3, 1-45). Tanagawa does not expressly disclose an SD memory card driven by said driver and having a data protecting function, wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, the count value is used as the initial value, and transfer data is kept secret using the random number, and wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output. However, Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65); Domenik teaches encrypting data using the random number (column 3, lines 1-52), and Hoffman teaches wherein said oscillator comprises a voltage-controlled oscillator having

an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output and said oscillator and said external terminal are electrically connected after the count value is output (column 3, lines 1-65); and Maeda teaches a random number generated by a SD memory card (figures 2A, 2B, 2C, 3A). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output and to keep transfer data secret using the random number, an SD memory card, and to keep data secret using a random number. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claims 52 and 65, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Tanagawa teaches wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 53 and 66, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Tanagawa teaches wherein the signal is a signal output from a

power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 54 and 67, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Tanagawa teaches wherein the signal is an operation start signal output from a controller (column 2, lines 9-20).

Regarding claims 55 and 68, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 54 and 67, respectively above. Furthermore, Tanagawa teaches wherein the operation start signal is output when the controller recognizes that a power supply is turned on (column 2, lines 50-67).

Regarding claims 56 and 69, the combination of Tanagawa, Hoffman, Domenik, and Maeda does not disclose expressly wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user. However, Examiner takes Official Notice that performing an operation triggered by a user is conventional and well known. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output a signal when a user performs an operation since Examiner takes Official Notice that it was conventional and well known.

Regarding claims 57 and 70, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Tanagawa teaches that the output occurs only when a high read signal is received (column 2, lines 40-54) and Domenik teaches wherein said oscillator

is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal (column 9, lines 30-67).

Regarding claims 59 and 72, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Hoffman teaches wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal (columns 1-4, figures 1, 3).

Regarding claims 60 and 73, the combination of Tanagawa, Hoffman, Domenik, and Maeda does not disclose expressly wherein after the count value is output, the clock is used as a system clock. However, Tanagawa teaches the clock being independent from the system clock (column 2, lines 9-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the clock as a system clock after the count value was output. One of ordinary skill in the art would have been motivated to do so because the use of system clocks was well known in the art.

Regarding claims 61 and 74, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Tanagawa teaches wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output (column 3, lines 25-40).

Regarding claims 62 and 75, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Domenik teaches using a latch circuit (column 6, lines 1-30).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because using a count value as initial or seed value for a random number generator was well known in the art.

Regarding claims 63 and 76, the combination of Tanagawa, Hoffman, Domenik, and Maeda teaches the limitations as set forth under claims 51 and 64, respectively above. Furthermore, Tanagawa teaches wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number generating circuit as the initial value (column 2, lines 40-67, column 3, lines 1-45).

11. Claims 6, 11, 18, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa and Hoffman, and further in view of Domenik.

Regarding claims 6 and 18, the combination of Tanagawa and Hoffman does not disclose expressly wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal. Tanagawa teaches that the output occurs only when a high read signal is received (column 2, lines 40-54). However, Domenik teaches wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal (column 9, lines 30-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value

is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because stopping processing after a result is output was well known in the art.

Regarding claims 11 and 23, the combination of Tanagawa and Hoffman does not disclose expressly comprising a latch circuit which latches the count value on the basis of the signal, wherein the count value latched by said latch circuit is used as the initial value. However, Domenik teaches using a latch circuit (column 6, lines 1-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because using a count value as initial or seed value for a random number generator was well known in the art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off on Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DGC

11/14/05
Primary Examiner
AU 2131